In the Specification:

Please amend page 7, paragraph 1, as follows:

In this case, the instruction adds two values together (R1 and R2) and stores the result in [[as]] R3. The values being added together, R1 and R2, are referred to as source operands, while R3 is referred to as the destination register. R1, R2, and R3 are architectural register pointers that do not have a fixed correlation with a physical register in the processor 2.

Please amend page 7, paragraph 3, as follows:

The first of these structures is the Free Physical Register Array 20 (FPRA) 20. The FPRA 20 is a memory structure that keeps track of P-A registers that are not being used, and are thus "free" or "soon-to-be-free"[[.,]] or available to be used as a destination register. The FPRA 20 therefore provides a physical register number for each instruction that requires a destination register. Once a physical register is assigned, or mapped, it is no longer considered "free" because it is now "in-use".

Please amend page 10, paragraph 1, as follows:

FIG. 3 is a flowchart illustrating the inventive memory structures tracking and recycling of physical registers. As stated above, the FPRA 20 tracks 64 of the 180 physical registers. The FPRA 20 and RPRM 22 memory structures are initialized for processing as shown in step 32. The FPRA 20 tags each of its physical registers as "free", meaning that they were currently available for use as a destination operand. The physical registers in FPRA 20 can also be tagged as "soon to be free", meaning that they are no longer in use and will soon be free once the speculative conditions which initiated the change in status are confirmed to be correct as shown as step 34. Once a physical register has been assigned as a destination operand by the FPRA 20, that register assignment information is moved to the APRM 22 as shown in step 36. Essentially, the APRM 22 tracks the physical register assignment information for instructions that are currently in the execution pipeline. The physical registers stored in the APRM 22 are marked as "in use, not yet retired" as shown in step 38.

Please amend page 10, paragraph 2, as follows:

The microprocessor 2 determines whether an instruction has retired from the execution pipeline as shown in step 40. If the instruction retires from the execution pipeline, the physical register assignment information moves from the APRM 22 to the RPRM 24 as shown in step 42. Otherwise, the APRM 22 maintains the physical assignment information. The RPRM 24 tracks physical register information for 116 registers. The physical registers in the RPRM 24 are essentially marked as "in-use, retired" as shown in step 44. Once an architectural register in the RPRM 24 is re-used as a destination register, the corresponding physical register is no longer "in-use". Subsequently, the physical register is moved from the RPRM 24 to the FPRA 20, and the FPRA 20 marks these physical registers as "soon to be free". When the architectural register is officially overwritten, the contents of the "soon-to-be-free" register in the FPRA 20 become obsolete and the physical register is then marked as "free". ~~Subseqently~~ Subsequently, this makes the physical register available for use by another instruction as shown in step 46.[[.]]